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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,378	MINE, KAZUMASA	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-35* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-35 have been considered. Claim 24 has been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 28 December 2005 and Extension of Time for Three Months as received on 28 December 2005.

Allowable Subject Matter

3. Claims 19-23 are allowed. Please see previous Office Action dated 30 June 2005 for reasons for allowance.

4. Claims 24-35 are allowed. The following is an examiner's statement of reasons for allowance: Claim 24 recites "updating said stack pointer in said stack memory in said coprocessor and said program counter in said coprocessor during an execution by said main processor." Prior art searched and cited has taught updating the stack pointer and program counter by the main processor when the main processor is executing the instruction. Prior art searched and cited has also taught that the co-processor updates the stack pointer and program counter prior or after it executes an instruction itself, but not when the main processor executes the instruction. The claim language states that the co-processor updates the stack pointer and program counter during instruction execution by the main processor, not by the co-processor before or after the co-processor executes the instruction.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 4-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Holmbo, U.S. Patent Number 4,860,200 (herein referred to as Holmbo).

8. Referring to claim 1, Levy has taught a microprocessor system for executing instructions described in a program comprising:

a. A main processor for executing, by hardware, instructions which belong to a first instruction set (Levy Abstract; column 2, lines 49-63; Figure 2; and Figure 3) and for executing, by software, instructions which belong to a second instruction set (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; and Figure 3); and

b. Said main processor including an interrupt request reception circuit (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7);

c. A co-processor operative under the control of said main processor for autonomously fetching an instruction belonging to said second instruction set to

execute same by hardware of said co-processor, (Levy Abstract; column 2, lines 35-63; column 8, lines 34-41; column 9, lines 42-46; Figure 2; and Figure 3);

d. Said co-processor including an interrupt request generation circuit, said interrupts request generation circuit being connected to said interrupt request reception circuit by at least one signal line and allowing an interrupt address to be identified in said main processor (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

9. Levy has not taught

a. To decode an interrupt vector for said execution of an instruction of said second instruction set by using an interrupt handler; and

b. Encoding said interrupt vector.

10. Holmbo has taught

a. To decode an interrupt vector for said execution of an instruction of said second instruction set by using an interrupt handler(Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2); and

b. Encoding said interrupt vector(Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2).

11. A person of ordinary skill in the art at the time the invention was made, and as taught by Holmbo, would have recognized that using vector interrupts decreases the delay caused by executing an interrupt (Holmbo column 2, lines 6-8), thereby increasing the speed and efficiency of interrupt execution. In regards to Holmbo, Holmbo has taught in the cited lines that executing an interrupt in the additional peripheral device that does not use interrupt vectors like the

processor in Holmbo's device causes a delay in executing the interrupt routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupt vectors of Holmbo in the device of Levy to increase the speed and efficiency of interrupt execution.

12. Referring to claim 2, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set which said co-processor cannot process by itself and issues a notification of said encounter to said main processor to thereby request the main processor to execute said specific instruction (Levy Abstract; column 9, lines 46-59; column 10 ,lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7).

13. Referring to claims 4-7 and 11, Levy has taught:

a. Wherein said co-processor issues said notification by dedicated interrupt assigned in advance respectively to a predetermined number of the instructions belonging to said second instruction set which have a higher frequency of execution than the other instructions (Applicant's claims 4) (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7)

b. Wherein said interrupt request reception circuit in said main processor encodes said dedicated interrupts sent from said co-processor (Applicant's claim 11) (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

14. Levy has not taught:

a. Interrupt vectors (Applicant's claim 4)

b. Wherein at least one of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5)

c. Wherein priorities are set to a plurality of said dedicated interrupt vectors (Applicant's claim 6)

d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7)

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11).

15. Holmbo has taught:

a. Interrupt vectors (Applicant's claim 4) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2)

b. Wherein at least one of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2). In regards to Holmbo, the interrupts react to interrupts that are occurring due to certain instructions in Holmbo's additional peripheral device.

c. Wherein priorities are set to a plurality of said dedicated interrupt vectors (Applicant's claim 6) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2);

d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2); and

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2).

16. A person of ordinary skill in the art at the time the invention was made, and as taught by Holmbo, would have recognized that using vector interrupts decreases the delay caused by executing an interrupt (Holmbo column 2, lines 6-8), thereby increasing the speed and efficiency of interrupt execution. In regards to Holmbo, Holmbo has taught in the cited lines that executing an interrupt in the additional peripheral device that does not use interrupt vectors like the processor in Holmbo's device causes a delay in executing the interrupt routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupt vectors of Holmbo in the device of Levy to increase the speed and efficiency of interrupt execution.

17. Referring to claims 8-10, Levy has taught wherein said co-processor further comprises:

a. A stack memory for holding data generated in the course of execution of an instruction which belongs to said second instruction set (Applicant's claim 8) (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3);

b. A stack pointer for holding an address of the most recent data in said stack memory (Applicant's claim 8) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12);

c. A hardware resource for carrying out a process for updating said stack pointer among processes which take place in the course of execution of said specific instruction (Applicant's claim 8) (Levy column 12, lines 26-31 and Figures 8-12);

d. A program counter for holding an address of an instruction which is currently processed and belongs to said second instruction set (Applicant's claim 9) (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7);

e. A hardware resource for carrying out a process for updating said program counter among processes which take place in the course of execution of said specific instruction (Applicant's claim 9) (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7); and

f. A status register for holding information indicative of a need of said notification and wherein said main processor periodically accesses said status register to recognize, from content of said status register, that said co-processor has encountered said specific instruction to thereby execute said specific instruction (Applicant's claim 10) (Levy column 5, lines 18-42; column 7, lines 29-64; column 8, lines 21-24; Figure 3; Figure 6; and Figure 7).

18. Referring to claims 12-16, Levy has taught

a. An instruction queue for holding a fetched instruction which belongs to said second instruction set (Applicant's claim 12) (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3);

b. Wherein said main processor refers to said instruction queue of said co-processor to specify an interrupt handler which corresponds to said specific instruction to be executed (Applicant's claim 12) (Levy column 9, lines 42-59; Figure 6; and Figure 7);

c. Wherein said co-processor includes a stack architecture (Applicant's claim 13) (Levy Abstract; column 5, lines 31-59; and Figure 3);

d. A stack memory provided outside said co-processor (Applicant's claim 14) (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3),

e. A stack-top register for holding a predetermined number of top data of stack data (Applicant's claim 14) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12);

f. A cache memory provided between said stack memory and said stacktop register for caching a part of data held in said stack memory (Applicant's claim 15) (Levy column 11, lines 1-14; Figure 3; and Figure 10); and

g. Wherein said co-processor detects a predetermined instruction for which stack data needs to be manipulated over said stack-top register and said stack memory (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12),

h. Whereupon said co-processor moves contents of said stack-top register to said stack memory (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-

12) and thereafter requests said main processor to execute said predetermined instruction (Applicant's claim 16) (Levy column 6, lines 50 to column 7, line 24), said main processor referring to contents of said stack memory, to which said contents of said stack-top register have been moved (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12), to thereby execute said predetermined instruction (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12). In regards to Levy, the example embodiment completes stack instructions in the co-processor, but, as is stated in column 6, line 50 to column 7, line 24 of Levy, the co-processor may send these instructions to the host.

19. Referring to claim 18, Levy has taught a program memory in which instructions belonging to said second instruction set are contained, wherein said co-processor further comprises:

a. A program counter for holding an address of an instruction that is currently processed and belongs to said second instruction set (Levy column 5, lines 8-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7);

b. An instruction queue for holding instructions which belong to said second instruction set (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3); and

c. An instruction fetch circuit for fetching an instruction belonging to said second instruction set from said program memory using a value contained in said program counter as its address and for setting the fetched instruction to said

instruction queue (Levy column 5, lines 8-42; column 7, lines 29-42; column 8, liens 34-41; column 9, lines 42-59; Figure 3; Figure 6; and Figure 7).

20. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Holmbo, U.S. Patent Number 4,860,200 (herein referred to as Holmbo), as applied to claim 2 above, and in further view of Irwin, U.S. Patent Number 4,695,945 (herein referred to as Irwin). Levy has not explicitly taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be handled to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself. However, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7). Irwin has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be handled to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Irwin Abstract; column 2, lines 39-64). A person of ordinary skill in the art at the time the invention was made, and as stated in Irwin, would have recognized that detecting this type of encounter is necessary to identify possible problems of contention for system resources (Irwin column 2, lines 22-24). By identifying these encounters, the processors resolve the resource contention and allow for processing to continue. Therefore, it would have been

obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the encounter detection of Irwin in the device of Levy to resolve resource contention.

21. Claims 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Holmbo, U.S. Patent Number 4,860,200 (herein referred to as Holmbo), as applied to claim 1 above, and in further view of Yamanaka, U.S. Patent Number 4,774,625 (herein referred to as Yamanaka). Levy has not taught a plurality of coprocessors in correspondence with a plurality of processes described in a program. Yamanaka has taught a plurality of coprocessors in correspondence with a plurality of processes described in a program (Yamanaka column 1, line 21 to column 2, line 28; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized that the plurality of coprocessors would allow for more operations to be executed simultaneously, thereby increasing speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the plurality of coprocessors of Yamanaka in the device of Levy to increase processor speed.

Response to Arguments

22. Applicant's arguments filed 28 December 2005 with regards to claims 1-18 have been fully considered but they are not persuasive. Applicant's arguments on pages 16-18 state in essence "...Applicant submits that the Examiner's description of Holmbo is a bit of a mischaracterization, since the mechanism in this secondary reference does not encode the vector interrupt information..." This has not been found persuasive. The claim language merely states "said co-processor including an interrupt request generation circuit for encoding said interrupt

vector". Encoding the vector interrupt merely means that the vector interrupt is converted into a given format or formatted according to a standard format (See accompanying definitions). The fact that the co-processor sends out a vector interrupt means that the co-processor has generated an interrupt in a format recognizable by both the main processor and co-processor, e.g. the co-processor has encoded an interrupt. Along these lines, the fact that the vector interrupt is represented by a series of 1's and 0's, as is standard for all computers, means that the vector interrupt has been encoded, since the states and code it has been converted into the standard computer recognizable format. Another interpretation is that the signals Holmbo describes in his specification in the sections cited in the rejection above set, in response to the interrupt, to properly process the interrupt is another type of encoding, since these signals are needed along with the original interrupt in order to properly process the interrupt vector. The interrupt signals are another type of format needed by the processors for interrupt execution.

23. Applicant's arguments state explicitly on page 17 the advantages of the specific encoder and decoder mechanism for the interrupts and explicitly states in paragraph 5 on page 17 "The advantage of this mechanism is that it permits the main processor to be able to immediately recognize the interrupt without having to take time to search memory for an interpretation of which set of instructions the co-processor to requesting the main processor to execute..." This is not in the claim language. As asserted earlier in the arguments, the claim language merely states "...encoding said interrupt vector" and nothing about immediately recognizing the interrupts without having to search memory for an interpretation. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., encoding means to make the interrupts immediately

recognizable without having to search memory for an interpretation) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Schmidt et al., U.S. Patent Number 5,715,439, has taught a main processor and co-processor system with transactions signaling which processor is to be executing.

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

26. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
3 March 2006

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